# Etch-Free Integrated III-Nitride Photonics via Bottom-Up Selective-Area Growth

**Minming He[1], Junho Park[1], Yifu Guo[1], Omar Alkhazragi[1,2], Jiangnan Liu[1], Liangqing Cui[1], Theodore Norris[1], Zetian Mi[1], and Di Liang[1]**

[1] *Electrical and Computer Engineering, University of Michigan, 1301 Beal Avenue, Ann Arbor, MI 48109, USA*
[2] *Electrical Engineering, King Fahd University of Petroleum and Minerals (KFUPM), Dhahran, Saudi Arabia*

[*] *liangdi@umich.edu*

**Abstract:** We demonstrate a selective-area growth for high-quality photonic integration, particularly on III-nitride platform for the first time. The reduced optical and likely lower electrical losses pave the way for broadband IR-visible-UV active-passive integration.

## 1. Introduction

III–Nitride (ultra)wide-bandgap materials enable bright LEDs, high-power laser diodes and other functional photonic devices across the IR, visible and UV bands [1,2] for various communication, sensing, quantum, and other emerging applications. There is growing research interest in developing advanced photonic integrated circuits (PICs) on III-N platforms [3–5]. The majority of PICs are based on *in-plane* waveguide devices for routing and manipulating light on-chip, typically fabricated through conventional top-down etching processes. In dry etched III-N structures, however, plasma damage and sidewall roughness inevitably introduce traps and optical scattering loss: both having increasingly negative impact at shorter wavelength [6]. Here to our best knowledge, we fabricate *in-plane* III-N photonic components and circuits by a bottom-up selective-area growth (SAG) technique for the first time. This etch-free process fixes the optical boundary crystallographically and avoids plasma damage.

## 2. Platform Design and Fabrication (SAG–MBE)

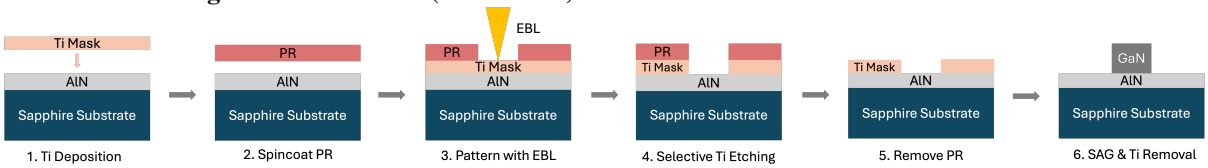


Fig. 1: Schematic bottom-up SAG fabrication flow.

In this proof-of-concept demonstration, we fabricated a simple single-crystalline PIC including GaN single-mode waveguide, microring resonators and grating couplers on sapphire substrate with a 500 nm thick AlN seed layer by molecular beam epitaxy (MBE). Fig.1 schematically shows the fabrication flow, starting from a blank deposition of 10 nm-thick Ti, followed by coating of the electron-beam lithography (EBL) resist. Upon completing the EBL process, device patterns were transferred to the 10 nm-thick Ti layer through a short and gentle dry etch. Lastly, selective-area MBE was performed on a clean, Ti mask-patterned sample as a "bottom-up" approach, enabling little sidewall roughness and precise control of GaN dimensions in contrast to the conventional "top-down" fabrication method. The microring design encodes a $5 \times 6$ (varied gap × bus) matrix at two radii (60 μm, 80 μm); same devices fabricated with conventional "top-down" approach were also characterized alongside to the bottom-up devices for direct comparison.

## 3. Results and Discussions

Devices were designed for TE-polarized operation at C-band, with tunable laser light coupled in and out through grating couplers. Lorentzian fits on measured spectra yield loaded $Q_L$ and extinction ratio, and intrinsic $Q_{\text{int}}$ is de-embedded when the device was near-critical and neighboring modes agree. The group index was extracted from the free spectral range (FSR) using $n_g = \lambda^2/(\text{FSR} \cdot L)$ where $L$ is the microring circumference. Propagation loss was estimated from $Q_{\text{int}}$ and corroborated by an independent spiral cutback measurement.

Fig. 2(a-c) are scanning electron microscopy (SEM) images of fabricated devices. The bottom-up flow produces etch-free, crystallographic sidewalls: the PIC chip top view (Fig. 2(a)) and zoom-in view of the bus-microring coupling region (Fig. 2(b)) show precise EBL-defined pattern transfer into GaN waveguide devices, while the close-up view in Fig. 2(c) reveals a smooth sidewall profile without plasma-etch roughness. The GaN surface roughness of RMS = 2 nm was measured using Atomic Force Microscopy, which is believed to contribute significantly to transmission loss. Growth optimization is on the way to achieving sub-nm surface roughness.

The focusing grating coupler exhibits a measured loss of 9.5 dB vs. simulated loss of 7 dB. The excess loss is attributed to GaN surface roughness, experimental uncertainty, and unaccounted link loss. Fig. 3(a) shows the broad transmission scan with a fine-scan inset revealing a near-critically coupled resonance with 17.1 dB extinction ratio and 2.5869 nm FSR. The device comprises a 1.05 μm-wide bus and microring (60 μm radius, 150 nm gap).

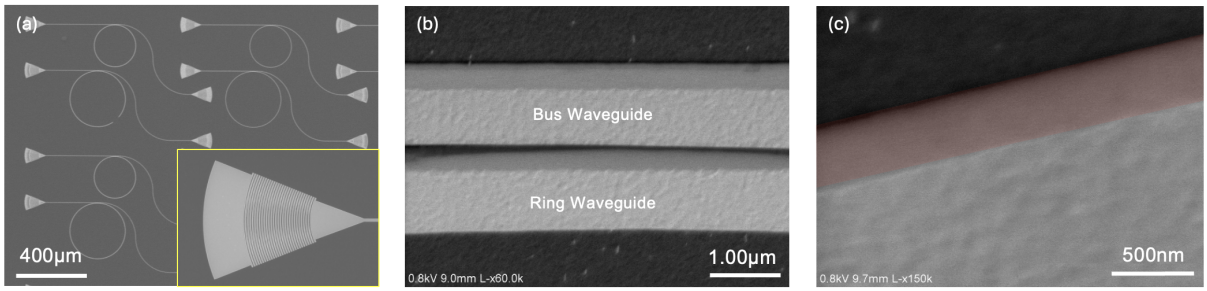


Fig. 2: SEM images of (a) MRR chip with grating-coupler close-up in the inset; (b) device coupling region; (c) close up of the sidewall, highlighted in red.

Lorentzian fitting gives loaded quality factor $Q_L = 13{,}030$ and intrinsic quality factor $Q_{\text{int}} = 35{,}124$. The extracted group index is $n_g$=2.34±0.01 across all devices, closely matching the simulated value of 2.37.

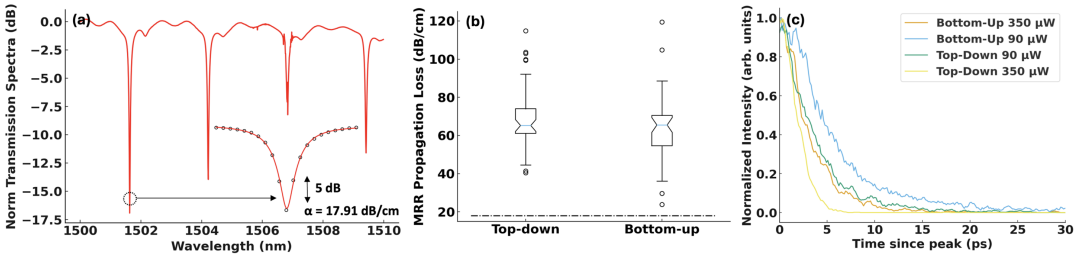


Fig. 3: (a) Normalized device transmission spectra. *Inset:* Lorentzian fit of the dip near 1502 nm; (b) Microring propagation-loss distributions of top-down vs. bottom-up (both radii combined) with cut back reference as dashed line; (c) Time-resolved decay time measured on both devices.

Extracted microring waveguide propagation loss distributions for top-down and bottom-up devices show similar median in Fig.3(b) , yet the *minimum* loss is much lower for bottom-up in both radii with lower 1st quartile. For the larger rings, the bottom-up spread is tighter at a comparable mean, but for the smaller rings, the spread broadens for bottom-up's, consistent with wurtzite-facet (hexagonal) prominence at tight bends of the rings. Cutback measurement on bottom-up spiral waveguide leads to 17.91 dB/cm single-mode waveguide propagation loss, which is overlaid as a baseline and lies close to the best bottom-up rings, corroborating that the lower loss floor stems from material/sidewall quality rather than fitting artifacts. No light transmission was measured on the same spiral waveguide fabricated by top-down flow, indicating much higher loss.

To evaluate electrical interface quality on etch-free and dry-etched samples, we also conducted time-resolved photoluminescence (TRPL) measurement under 268 nm excitation at two power levels (90 and 350 µW). Longer decay time for the bottom-up devices was observed at both powers in Fig. 3(c). Longer lifetimes indicate likely reduced nonradiative recombination, fewer mid-gap defects and/or lower surface recombination velocity [7], consistent with the smooth sidewalls and the lower achievable optical loss floor. Further measurements are underway to verify that this trend is not dominated by surface-induced polarization fields. Given that the bottom-up and top-down devices share the same nominal dimensions from the same mask layout, any surface-induced field should be comparable across both. Therefore, the systematically longer lifetimes in the bottom-up devices suggest that the improvement is unlikely to be an artifact of trap filling at low excitation, but instead reflects a genuine enhancement in interface quality. These results are fully aligned with expectations that defect density and surface damage are inherently reduced in an etch-free, bottom-up growth process.

## 4. Summary

For the first time, we demonstrated a "bottom-up" SAG approach to fabricate high-quality in-plane single-crystalline photonic components. This etch-free approach smooths out the sidewalls crystallographically, reducing sidewall roughness and etch damages effectively. On-going effort to further extend this etch-free platform to visible and UV wavelengths, particularly to integrate with our recently developed world-first single-frequency UV diode laser [8], will make the approach a credible foundation for high-quality passive and active devices towards scalable III–N PICs. It has the potential to become a generic monolithic integration approach for materials with c-axis-favored epitaxy, e.g., Wurtzite (ZnO) or Hexagonal ($\varepsilon$-$Ga_2O_3$) .

**References:** [1] S.-Z. Zhao *et al.*, *Sci. Rep.* **5**, 8332 (2015); [2] C. Xiong *et al.*, Int. J. High Speed Electron. Syst. **23**, 1450001 (2014); [3] N. Bhat *et al.*, Opt. Mater. Express **14**, 792–800 (2024); [4] J. Yan *et al.*, IEEE Trans. Electron Devices **71**, 3056–3061 (2024); [5] C. Shen *et al.*, in CLEO-PR, paper S2520 (2017); [6] H. Chen *et al.*, *Opt. Express* **25**(25), 31758–31773 (2017); [7] J. Mickevicius *et al.*, *Appl. Phys. Lett.* **87**(24), 241918 (2005); [8] O. Alkhazragi *et al.*, presented at the *IEEE Photonics Conference*, Singapore (2025).